AHIP-370

Advanced High Integration Platform with PPGA Celeron® Processor

P/N 350370(B)

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Chapter 1 Introduction

Product Overview

The Xycom Automation Advanced High-Integration Platform 370 (AHIP-370) board is developed expressly for use in Xycom's line of flat panel industrial personal computers. It is based on the AHIP6 but is optimized in design, layout, and features for use with flat panel computer systems. This integrated design approach allows Xycom industrial PC/ATs to incorporate "Big PC" features in an extremely compact package. These "Big PC" features include AGP video PCI/ISA expansion, Celeron CPU, full-size hard disk, status LEDs, infrared port, and integrated touchscreen.

Module Features

- Supports
  - 66 MHz and 100 MHz front side bus
  - Intel Celeron® processors (PPGA package)
- 32 MB - 256 MB DRAM DIMMs
- AGP local bus XGA graphics with 2 MB integrated DRAM
  - Up to 1024x768\256 colors non-interlaced
  - 640x480x256K, 800x600x64K, 1024x768x256 color TFT panels
- PCI fast IDE controller
- Two 16550-compatible serial ports
  - COM 1 is RS-232, or RS-485
  - COM 2 is RS-232 port, or Infrared (IR or IrDA), or Touchscreen
- Centronics-compatible parallel port
- Floppy Controller (only one floppy supported)
  - Internal FFC connector
  - External connector
- Touchscreen interface (COM 2 or PS/2 mouse port)
- PS/2 keyboard port
- Real time clock and battery
- Disk on a chip supported (DOC 2000)
- 32Kx8 and 128Kx8 nonvolatile RAM supported
- LED interface
- Designed specifically for Xycom Automation industrial PC/ATs.

Architecture

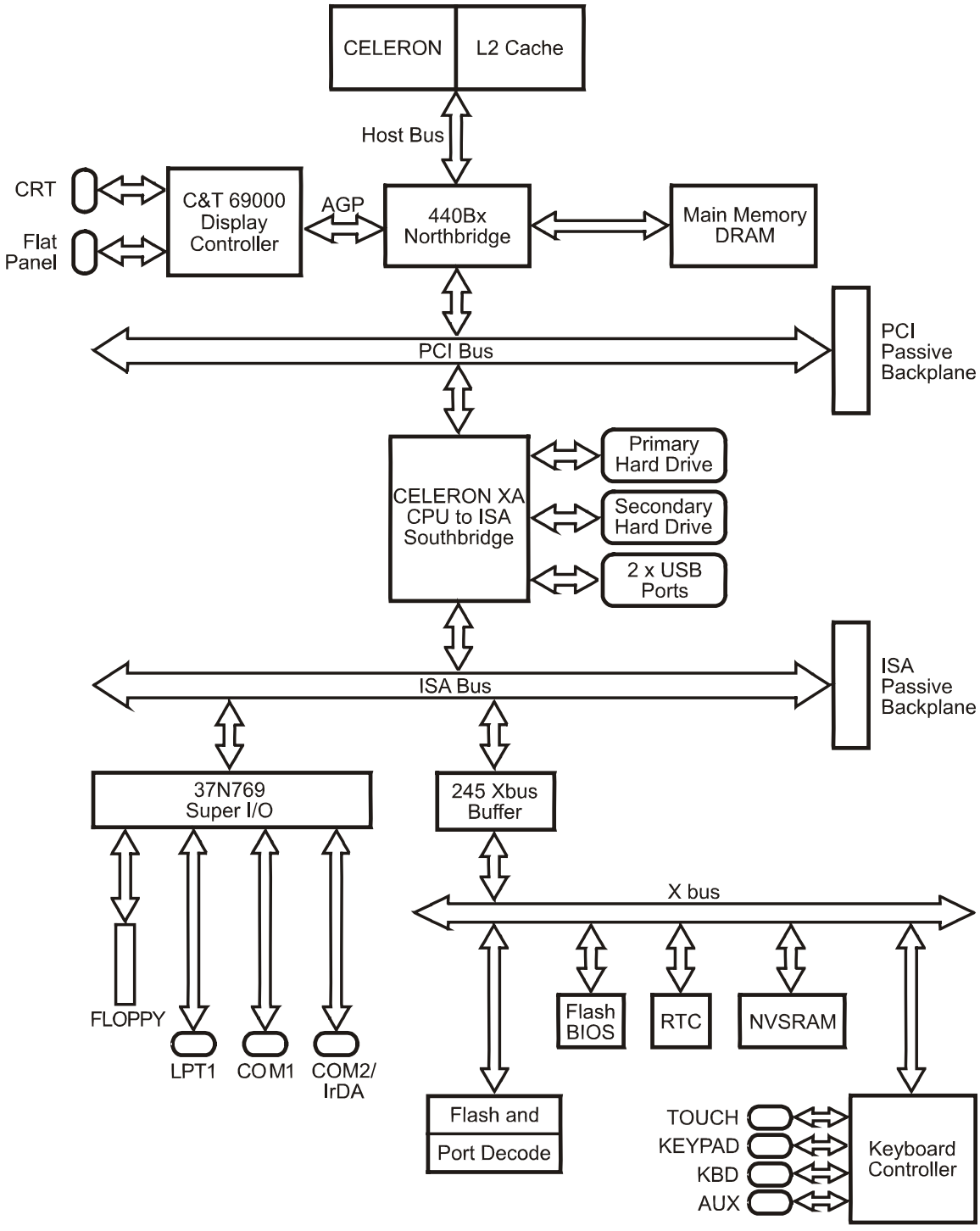

Figure 1-1. AHIP-370 Block diagram

Local Bus Interfaces

The Celeron design uses the 440BX chip set. The 440BX integrates a high performance interface from PCI to IDE. This interface is capable of accelerated data transfers.

The 440BX chipset provides an accelerated PCI-to-ISA interface that includes

- A high-performance enhanced IDE controller
- PCI and ISA master/slave interfaces
- Plug-and-play port for on-board devices

The chipset also provides many common I/O functions found in ISA-based PC systems, including:

- Seven-channel DMA controller
- Two 82C59 interrupt controllers
- 8254 timer/counter
- Control logic for NMI generation

Fast IDE controller

The high-speed local bus IDE controller supports programmed I/O modes 0-4. It also provides 4x32-bit read-ahead buffer and 4x32-bit write-post buffer support to enhance IDE performance.

Accelerated Graphics Port (AGP)

XGA Graphics Controller

The AGP bus controller supports CRT displays and flat panel displays with 2 MB video memory. The controller also supports resolutions of 640x480, 800x600, and 1024x768 with 64K colors.

Note

The IDE controller supports enhanced PIO modes, which reduce the cycle times for 16-bit data transfers to the hard drive. Check with your drive manual to see if the drive you are using supports these modes. The higher the PIO mode, the shorter the cycletime.

Select the PIO modes in the BIOS setup (refer to Chapter 3). The autoconfigure classifies the drive connected if the drive supports the auto ID command. If you experience problems, change the PIO to standard.

On-board Memory

DRAM

The AHIP-370 has two 168-pin DIMM memory sites, providing up to 256 MB of SDRAM (with up to 512 MB capability in the future). The memory site is populated by 100 MHz synchronous DRAM.

Flash BIOS

The AHIP-370 board uses a Flash BIOS. Flash is used for system BIOS and video BIOS.

Non-volatile SRAM

The AHIP-370 hardware supports non-volatile SRAM. Contact Xycom Automation at 1-800-AT-XYCOM (1-800-289-9266) for additional information about this feature.

The SRAM comes in a module type package and contains a built-in battery and battery backup circuitry. The battery life is approximately seven years in the absence of VCC. The SRAM supports 32Kx8 and 128Kx8 memory sizes. The RAM comes in a 32 pin dip (0.6 inches wide) standard format.

SRAM can be located at: CC000, D0000, or D8000.

DiskOnChip 2000

The DiskOnChip 2000 is a single-chip Flash disk in a standard 32-pin DIP format. It requires an 8 Kbyte window to view as an extension BIOS. During boot up, the DiskOnChip loads its software in the PC's memory and installs itself as an additional drive.

Serial and Parallel Ports

PC/AT peripherals include two high-speed, RS-232, 16550-compatible serial ports and one bi-directional Centronics-compatible parallel port:

- COM 1 of the serial ports accepts either RS-232 or RS-485 connections.
- COM 2 is RS-232 (stacked DB 25) with parallel port.

The COM2 port can be used for one of three options:

- Serial port out the 25 pin DB connector
- Touchscreen controller interface
- Infrared (IrDA) interface

The BIOS setup is used to configure the port as a serial port or IrDA port. This port can be used as both a serial interface and an IR interface, by allowing software to control the connection.

If the touchscreen controller is jumpered to use COM2, the 25-pin DB connector must not be used to interface to a device. These lines are combined internally. The BIOS setup menu for COM2 must be set to standard operation to use the touchscreen controller on COM2.

USB

USB (Universal Serial Bus) is a "plug-and-play" interface between a computer and add-on devices (such as audio players, joysticks, keyboards, telephones, scanners, and printers). With USB, a new device can be added to your computer without having to add an adapter card or even having to turn the computer off. USB supports a data speed of 12 megabits per second. This speed will accommodate a wide range of devices, including MPEG-2 video devices, data gloves, and digitizers.

Keyboard Interface

The keyboard interface uses a standard PS/2-style connector. A polyswitch protects the +5 V. This device opens if the +5 V is shorted to GND. Once you remove the shorting condition, the polyswitch allows current flow to resume.

Hard and Floppy Drives

The floppy interface supports one floppy drive. The AHIP-370 can interface to a floppy via the on-board floppy connector or the external floppy connector.

In order to connect a floppy drive to the external connector after power up, the floppy drive must be setup for a 1.44 MB drive and the floppy drive test must be dis-

abled. If this is not done the system generates a floppy drive error during the POST (Power On Self Test).

The enhanced IDE (EIDE) interface supports up to 2 hard drives. Hard drive interface is via the Xycom plug-in backplane or the on-board IDE controller.

Caution

The higher the PIO mode, the shorter the cycletime. As the IDE cable length increases, this reduced cycle time can lead to erratic operation. The total IDE cable length must not exceed 18 inches. If two IDE drives are connected, they must not be more than six inches apart.

Environmental Specifications

Table 1-1. Environmental Specifications

Characteristic	Specification
Temperature	
Operating	0° to 55° C (32° to 140° F)
Non-operating	-40° to 85°C (-40° to 185°F)
Humidity	
Operating	20% to 80% RH noncondensing
Non-operating	20% to 80% RH noncondensing
Altitude	
Operating	Sea level to 10,000 feet (3048 m)
Nonoperating	Sea level to 50,000 feet (15240 m)
Vibration [a] (3512, 3515 systems [b])	
Operating	5 to 55Hz 0.006" peak to peak displacement 56-2000 Hz 1.0g maximum acceleration
Nonoperating	5-55 Hz 0.006" peak to peak displacement 56-2000 Hz 2.5 g maximum acceleration
Shock [a] (3512, 3515 systems [b])	
Operating	15g peak acceleration, 11 msec duration
Nonoperating	30g peak acceleration, 11 msec duration

[a] These values are with solid state hard drives and NOT rotating media drives

[b] Consistent with system level specifications. See your system manual if you have a system other than the 3512 or 3515 models.

Hardware Specifications

Table 1-2. Hardware Specifications

Characteristic	Specification
Power Specifications: The CPU power supply on the AHIP-370 provides a voltage range of 1.30V to 2.05V in increments of 50mV. The CPU selects its voltage through its four outputs VID3-VID0. The supply was changed to accommodate future Socket370 CPUs which will run at lower voltages.	The maximum current that the supply can deliver is 19A.
CPU speed	300 MHz, 366 MHz, and 433 MHZ
AGP Super VGA Graphics Controller	640x480, 800x600, and 1024x768, 64K colors maximum resolution 2 MB video DRAM
Serial Ports (2)	COM1 is RS-232 or RS-485 COM2 is RS-232, or IR, or Touchscreen Both 16550 compatible
Parallel Interface	Centronics compatible
On-board memory	Up to 256 MB; 66 MHz SDRAM

Chapter 2 – Installation

This chapter provides information on configuring the AHIP-370 Processor Module. Pinouts for the connectors are located in Appendix C.

Figure 2-1 illustrates the jumper and connector locations on the AHIP-370.

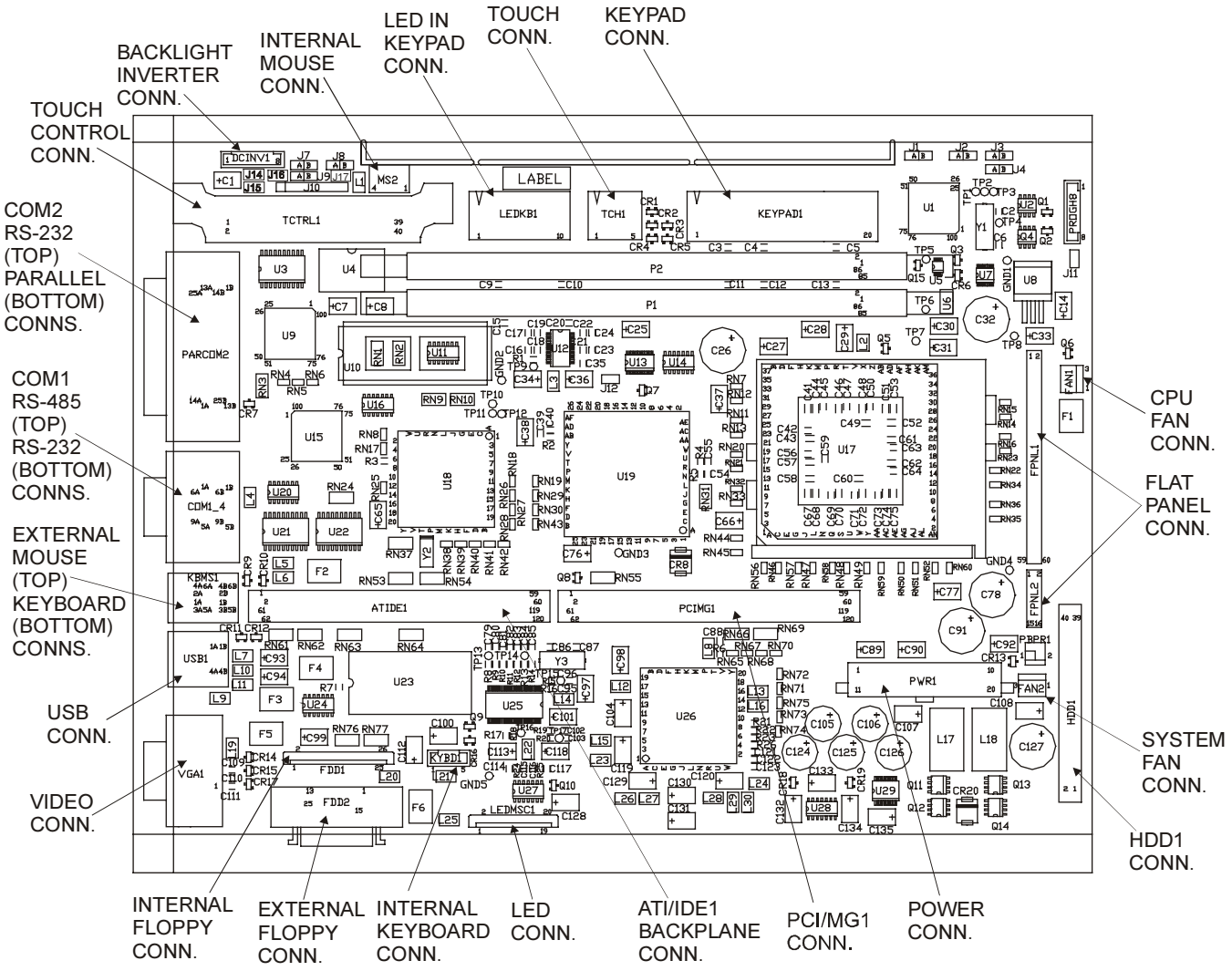

Figure 2-1. AHIP-370 Jumper and Connector Locations

Configuration Options

Jumpers

The following tables list AHIP-370 jumpers, their default positions and their functions. The jumpers marked “Access” are placed at the top of the board for easy customer access.

Table 2-1. AHIP-370 Jumpers

Jumper	Position	Function
J1	A	Push button reset switch DISABLED (Access)
	B	Push button reset switch ENABLED
J2	A	CMOS OK (Access)
	B	Clear CMOS
J3	A	Flat panel selected (Access)
	B	CRT selected
J4	A	Normal
	B	Program the H8
J7	A	Boot flash enabled
	B	Boot ROM enabled
J8	A	Enables RS-485 port in the assertive state.
	B	Enables RS-485 port in the negated state.
J9	A	DTR used to control the RS-485 port
	B	RTS used to control the RS-485 port
J18	A	VGA ENABLED
	B	VGA DISABLED

The BIOS recovery scheme used on the AHIP6 utilizes a jumper (J5) to select recovery mode. The Flash Programmable Gate Array (FPGA) at U15 uses this to define the state of address signal A18 into the flash chip. According to the following table:

J5*	Mode	Flash A18 state
A	Normal	Inverted
B	Recovery	Not Inverted

*Recent changes in flash technology have mandated that J5 be in the B position for normal operation. This is confusing, as it is contrary to the design documentation and user manual. Because of this, J5 has been eliminated on the AHIP-370. A 1K pull-down resistor is connected to signal XD (4) to simulate the B position.

The following table outlines the changes in jumper configurations between the AHIP-370 and AHIP6:

Table 2- 2. Changes in Jumper Configuration

AHIP6 Jumper	AHIP-370 Jumper	Description	Comments
J6	N/A	Controls the speed of the CPU	The socket370 implementation by Intel calls for the CPU to define its own speed and not be determined by jumpers. There are no jumpers on the AHIP-370 for this purpose.
J1	J1	A PB reset disabled B PB reset enabled	PB refers to an external pushbutton that may be connected through the RS-232 interface.
J2	J2	A CPU will not clear CMOS on power up B CPU will clear CMOS	
J3	J3	A Flat panel enabled B CRT port enabled	
J4	J4	A Normal operation B Puts H8 in program mode	
J5	N/A	A Normal flash boot B Recovery flash boot	See above.
J7	J7	A CPU boots from flash B CPU boots from ROM	
J18	N/A	A Onboard video enabled B Onboard video disabled	The video is always enabled on the AHIP-370. If an external VGA adapter is plugged into the system, the BIOS will disable the onboard chip.
N/A	J8	A The asserted state will enable the RS-485 port. B The negated state will enable the RS-485 port.	Refers to the state of the modem control signal selected by J9.
N/A	J9	A DTR is used to control the RS-485 port. B RTS is used to control the RS-485 port.	J8 and J9 function together to control the RS485 port. RS-485 TriState Control On the AHIP6, the RS-485 is enabled by asserting DTR. Two jumpers were added to the AHIP-370 to allow either DTR or RTS to control the RS-485 drives and determine whether the asserted or negated state will enable it.
J8	J10	Used to program Lattice component.	Factory use only.
NA	J14, 15, 16, 17	IN= Microtouch Controller OUT= Berguist Controller	These jumpers allow the PS2 AUX port and interlink mouse to pass through the Berquist controller.
J19	J11	Connecting the two pins will reset the CPU.	Factory use only for emulators.

N/A	J12	Forces front-side bus to run at 66MHz.	Factory use only.

All AHIP-370 jumpers are factory set in the "A" position.

System Interrupts

The following table describes the interrupts used on the AHIP-370.

Table 2- 3. System Interrupts

Interrupt	Function
IRQ0	System Timer
IRQ1	Keyboard
IRQ2	Cascade
IRQ3	Serial Port*
IRQ4	Serial Port*
IRQ5	Parallel Port*
IRQ6	Floppy Controller
IRQ7	Parallel Port*
IRQ8	Real Time Clock
IRQ9	Unused
IRQ10	Serial Port*
IRQ11	Serial Port*
IRQ12	Mouse Port
IRQ13	Math Co
IRQ14	Fixed Disk
IRQ15	Unused

* BIOS setup controlled

The BIOS setup menu controls the interrupts for the serial and the parallel port.

The two Serial ports on the AHIP-370 board can be mapped to any two of the following interrupts: 3, 4, 10, & 11 (defaults are interrupts 3 and 4). One parallel port can be mapped to IRQ5 or IRQ7. The BIOS setup menu is used to control the location and interrupts for the serial and parallel ports.

Note

The BIOS controls the mapping of the AGP interrupts to AT-bus interrupts. This means if a AGP device is plugged into a slot and needs an interrupt, one of the AT-bus interrupts must be mapped to the AGP interrupt.

DMA Mapping

Table 2-4. DMA Channels

DMA	Function
DMA0	Unused (Could be used for EPP/ECP parallel port option)
DMA1	Unused
DMA2	Floppy Controller
DMA3	Unused (Could be used for EPP/ECP parallel port option)
DMA5	Unused
DMA6	Unused
DMA7	Unused

DMA channels 0-3 are 8-bit and DMA channels 5-7 are 16-bit. When the ECP option is enabled, one of the 8-bit DMA channels is used.

Memory Map

The following table shows the AHIP-370 memory map. The I/O designation refers to memory viewed as part of the AT bus.

Table 2- 5. Memory Map

Address Range (HEX)	Size	Device
FFFE0000 - FFFFFFFF	128K	SYSTEM BIOS
end of DRAM - FFFDFFFF	xxxK	I/O Memory
00100000 - end of DRAM	xxxK	DRAM*
000F0000 - 000FFFFF	64K	SYSTEM BIOS
000E0000 - 000EFFFF	64K	SYSTEM BIOS
000D0000 - 000DFFFF	64K	AT bus I/O
000C0000 - 000CBFFF	48K	VGA BIOS
000A0000 - 000BFFFF	128K	VGA DRAM MEMORY
00000000 - 0009FFFF	640K	DRAM

*See Intel 430BX data sheet for a description of optional settings for assigning memory holes or gaps within memory map area.

I/O Map

The I/O map for the AHIP-370 in Table 2- 6 contains all the I/O ports of the IBM AT architecture with some additions.

Table 2- 6. I/O Map

Hex Range	Device
000-01F	DMA controller 1, 8237A-5 equivalent
020-021	Interrupt controller 1, 8259 equivalent
022-024	Available
025-02F	Interrupt controller 1, 8259 equivalent (see Note 3)
040-05F	Timer, 8254-2 equivalent
060-06F	8742 equivalent (keyboard)
070-07F	Real Time Clock bit 7 NMI mask (see Note 3)
080-091	DMA page register (see Note 3)
092	Reset/ Fast Gate A20
93-9F	DMA page register (see Note 3)
0A0-0BF	Interrupt controller 2, 8259 equivalent (see Note 3)
0C0-0DF	DMA controller 2, 8237A-5 equivalent (see Note 3)
0F0	N/A
0F1	N/A
0F2-0F3	N/A
0F4	IDE ID port
0F5-0F7	N/A
0F8	IDE Index port
0F9-0FB	N/A
0FC	IDE Data port
0FD-0FF	N/A
100	Available
102	C&T Global enable register
103-179	Available
180-181	SRAM control register (May be remapped based on I/O port 234h)
182-1EF	Available
1F0-1F7	IDE Controller (AT Drive)
1F8-22F	Available
231	Xycom LED port
233	Xycom Flash control register
234	Xycom IO port control register
278-27F	Parallel Port 2 (see Note 1)
280-2F7	Available
2F8-2FF	Serial Port 2 (see Note 1)
300-36F	Available
370-377	Alt. Floppy Disk Controller (see Note 1)
378-37F	Parallel Port 1 (see Note 1)
380-3AF	Available
3B0-3BB	mono mode video

Hex Range	Device
3BC-3BF	reserved for parallel port
3C0-3CF	VGA registers (see Note 2)
3D0-3DF	CHIPS flat panel & color mode registers
3E0-3EF	Available
3F0-3F7	Primary Floppy disk controller
3F8-3FF	Serial port 1 (see Note 1)
CF8	AGP configuration address register (see Note 4)
CFC	AGP configuration data register (see Note 4)

Note 1

Since serial and parallel port addresses can be changed or the port may be disabled, these addresses can be used for some applications and not for others.

Note 2

Reference the C&T69000 advance data book for detailed information.

Note 3

Reference the Intel 430BX chip set data book for detailed information.

Note 4

Reference the following for AGP configuration: AGP local bus specification rev 2.1, Intel 430BX chip set data book, and C&T69000 data book.

Registers

The AHIP-370 contains five I/O ports: 231h, 233h, 234h, and a user-definable port (port 180/1h, 2E0/1h, 3E0/1h, or 300/1h). These ports are compatible with AHIP4+ and AHIP 6+.

Register 231h – Miscellaneous Control

Register 231h controls the LEDs and signals shown in the following table.

Table 2- 7. Register 231h - CPU LED Port

Bit	LED/Signal	Result	R/W
0	Reserved	0	R
1	DOC 2000	1= Enables DOC 2000	R/W
2	Reserved	0	R
3	Reserved	0	R
4	Reserved	0	R
5*	ENFLASHWR	1 = Enables Flash write	R/W
6	VGA_EN	1 = Enables on-board VGA	R
7	CLRCMS	1 = CMOS okay 0 = Clear CMOS	R

*Note: This bit must be 1 to make FLASH visible @D0000h when booting from AT bus. This bit also enables the FLASH @C0000h when booting to FLASH.

Register 233h – Flash BIOS Control

Register 233h controls the signals shown in the following table.

Table 2- 8. Register 233h - Flash BIOS Control Register

Bit	Signal	Result	R/W
0	FLA15	Flash address 15 - page control bit	R/W
1	FLA16	Flash address 16- page control bit	R/W
2	FLA17	Flash address 17 - page control bit	R/W
3	FLA18	Flash address 18 - page control bit	R/W
4	FPSEL0	Flat panel select bit 0	R
5	FPSEL1	Flat panel select bit 1	R
6	FPSEL2	Flat panel select bit 2	R
7	FPSEL3	Flat panel select bit 3	R

Register 234h - I/O Port Location

Register 234h controls the I/O port location register shown in the following table.

Table 2- 9. Register 234h - I/O Port Location Register

Bit	Signal	Result	R/W
0	Reserved	0	R
1	Reserved	0	R
2	Reserved	0	R
3	Reserved	0	R
4	I/O range select	I/O range select bit 0	R
5	I/O range select	I/O range select bit 1	R
6	I/O port bit 0	I/O port bit 0	R/W
7	I/O port bit 1	I/O port bit 1	R/W

Bits 0-3 are reserved for the temperature sensor. Bits 4 and 5 are reserved for setting the memory location for the SRAM.

I/O Range Select

The following are ranges defined by register 234h.

Table 2- 10. I/O Range Selection

I/O range selection	Range
00	no range
01	CC000-CFFFF
10	D0000-D7FFF
11	D8000-DFFFF

Offset Registers

The following registers are located starting at the I/O location defined by register 234h.

Table 2- 11. I/O Port Selection (Port Address)

I/O port selection	Port address
00	180h
01	2E0h
10	3E0h
11	300h

Offset 0 Page Register for Programming (Port Address)

Offset 0 is a read-only register that checks the battery status

Table 2- 12. Offset 0 Page Register for Programming (Port Address)

Bit	Signal	Result	R/W
0	Battery status	0 = battery good 1 = battery fail	R
1	Reserved	0	R
2	Reserved	0	R
3	Reserved	0	R
4	Reserved	0	R
5	Reserved	0	R
6	Reserved	0	R
7	Reserved	0	R

Offset 1 Page Register for Programming (Port Address +1)

Offset 1 controls the paging bits for the ROM. This feature is needed for programming flash.

Table 2- 13. Offset 1 Page Register for Programming (Port Address +1)

Bit	Signal	Result	R/W
0	Control ROM/RAM15	ROM address 15-page control bit	R/W
1	Control ROM/RAM16	ROM address 16-page control bit	R/W
2	Control ROM/RAM17	ROM address 17-page control bit	R/W
3	Reserved	0	R
4	Reserved	0	R
5	Reserved	0	R
6	Reserved	0	R
7	Reserved	0	R

Connectors

This section describes the connectors for the AHIP-370. *Appendix C provides the pinouts for each of the connectors.*

Parallel Port Connector (PARCOM2)

The parallel port is a stacked DB 25-pin connector.

Serial Port Connectors

There are two serial ports supported on the AHIP-370 board.

COM1 Connector (COM1)

The COM1 is a nine pin connector consisting of two connectors attached to one logical port. Only one connector can be used at a time, either the RS-232 port or the RS-485 port.

COM2 Connector (PARCOM2)

The COM2 connector is a male DB 25-pin connector. This port can be used for three separate devices (but only one at a time):

- Touch screen controller
- IrDA interface
- LPT1/COM2 RS-232 connector

The BIOS setup determines whether the COM2 is used for the RS-232 connector or the IR interface. Jumpers on the touchscreen controller select the COM2 port or the auxiliary port. If a touchscreen controller is jumpered for COM2, this COM port is not available.

PS/2 Keyboard/Mouse Connector (KBMS1)

This double stacked connector provides an upper and lower connector for the keyboard and mouse port.

Internal Keyboard Connector (KYBD1)

This is a five-pin internal keyboard connector on the motherboard.

VGA (Video) Connector (VGA1)

The VGA (Video) connector is a 15-pin connector located on the I/O panel. This connector is only enabled when J3 is in position B or no flat panel is connected to the CPU board.

Floppy Drive Connector (FDD1 and FDD2)

There is an internal floppy connector (FDD1) and an external floppy connector (FDD2). The floppy interface supports only one floppy drive. The floppy drive connector is a 26-pin connector. Both of these ports use a polyswitch to protect VCC from directly shorting to GND.

Internal Mouse Connector (MS2)

This four-pin connector provides a future method to integrate a mouse to the front panel.

Internal LED Connector (LEDMSC1)

This 20-pin connector provides a low cost method to add LED’s to the touch only units, and also provides the pinout for the IR interface port.

LED In Keypad Connector

This connector is used for future designs that support the LEDs in the keypad.

ISA/IDE Backplane Connector (ATIDE1)

The ISA/IDE Backplane connector is a 120-pin connector. This connector provides both ISA and IDE signals to the backplane.

IDE Connector (HDD1)

IDE hard drive connector is a 40-pin header. This header is intended for future options and testing.

Power Connector (PWR1)

This 20-pin connector is a standard ATX style PC power supply connector.

Touch Control Connector (TCTRL1)

This 40-pin connector supports 5-wire touchscreens. The connector is latching to provide for a DRAM SIMM type installation.

Touch Connector (TCH1)

The five-pin touch connector is the interface to the touch panel.

Flat Panel Connector (FPNL1 and FPNL2)

The flat panel connector is a 60pin SMD through board connector. The four flat panel select lines define up to 16 unique panel types. If all signals are high (no cable attached) the system defaults to CRT.

The system board supports +5V and 3.3V TFT panels with a custom flat cable. It supports STN panels with a 2.5” X 2.75” PCB which contains the DC/DC for the custom VEE voltage along with the contrast and power sequencing circuit. There are also provisions to support a temperature sensor for automatic contrast control.

Backlight Inverter Connector (DCINV1)

This 8-pin connector provides power for the backlight inverter.

Chapter 3 – BIOS Setup Menus

The AHIP-370 board's customized BIOS is designed to surpass the functionality provided for normal PC/ATs. This custom BIOS allows you to access the value-added features on the AHIP-370 module without interfacing to the hardware directly.

Moving through the Menus

General instructions for navigating through the screens are described below:

Key	Result
F1 or ALT-H	General Help window
F2	Enters the menu
ESC	Exits the menu
← or → arrow keys	Selects a different menu
↑ or ↓ arrow keys	Moves the cursor up or down
TAB or SHIFT + TAB	Cycles the cursor up or down
HOME or PGUP	Moves the cursor to the top of the window
END or PGDN	Moves the cursor to the bottom of the window
F5 or -	Selects the previous value for the field
F6 or + or SPACE	Selects the next value for the field
F9	Loads the default configuration values for the menu
F10	Saves and Exits
ENTER	Executes the Command or Select ► Submenu or displays a pop up menu
ALT-R	Refresh screen

Note

An asterisk (*) indicates fields which may or my not be visible (depending on the option selected different fields may appear).

To select an item, use the arrow keys ↑↓ ←→ to move the cursor to the field you want. Then use the + and - keys to select a value for that field. For many fields, pressing ENTER displays a pop-up menu of all valid choices for the field.

An "►" beside a field indicates the presence of a submenu. To enter the submenu, use the arrow keys to select the field and then press ENTER.

BIOS Main Setup Menu

You start the BIOS Setup utility as your system boots up. To access the main menu, press F2 after the memory tests and before your system loads the operating system. If the Boot Time Diagnostic Screen (in the Advanced Menu) is enabled on your system, the BIOS will display the following message: "Press F2 to enter Setup."

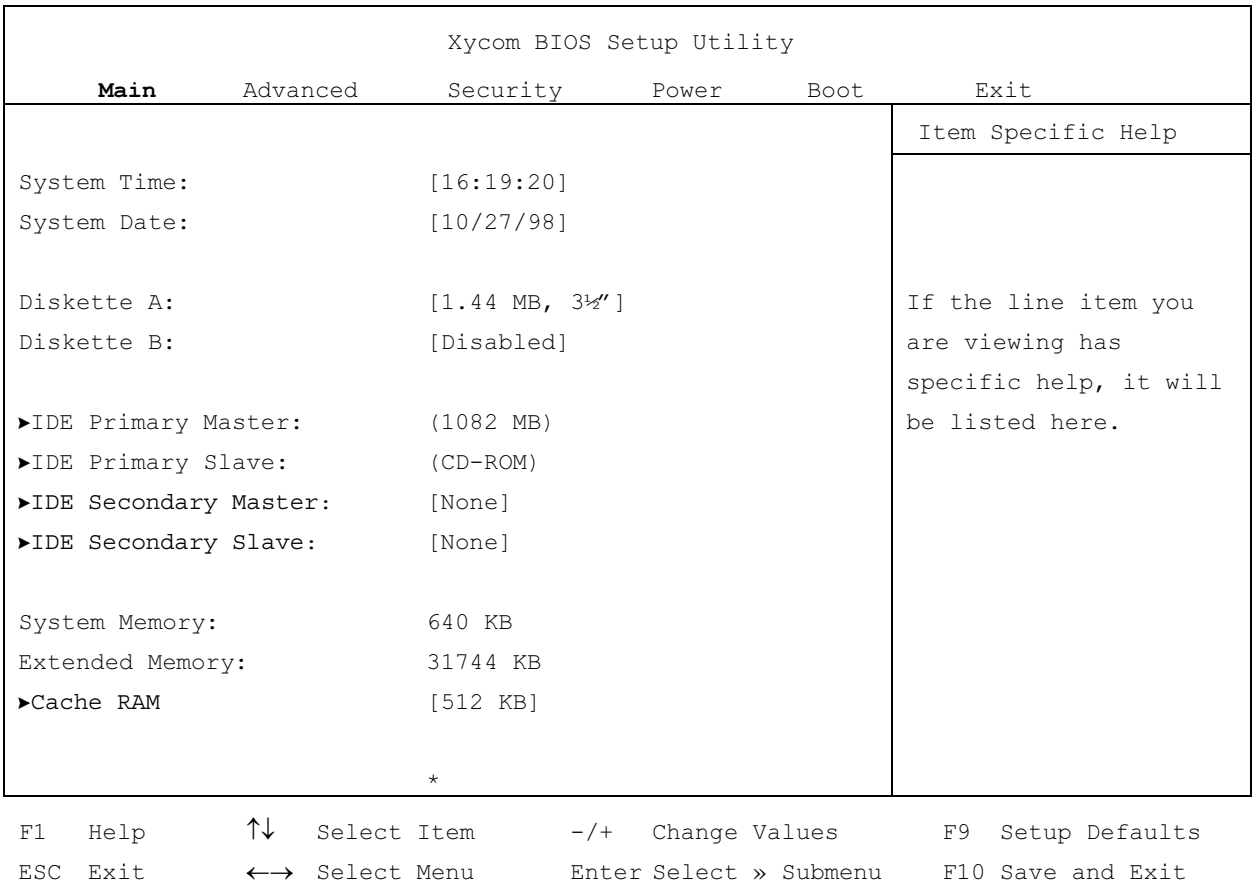
Xycom BIOS Setup Utility
Main Advanced Security Power Boot Exit
Item Specific Help
System Time: [16:19:20]
System Date: [10/27/98]
Diskette A: [1.44 MB, 3½"]
Diskette B: [Disabled]
If the line item you are viewing has specific help, it will be listed here.
►IDE Primary Master: (1082 MB)
►IDE Primary Slave: (CD-ROM)
►IDE Secondary Master: [None]
►IDE Secondary Slave: [None]
System Memory: 640 KB
Extended Memory: 31744 KB
►Cache RAM [512 KB]
*
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Save and Exit

Figure 3-1. Main Setup Menu

Table 3-1. Main Setup Menu Options

Option	Description
System Time (HH/MM/SS)	Sets the real-time clock for hour, minute, and seconds. The hour is calculated according to a 24-hour military clock (i.e., 00:00:00 through 23:59:59). Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to enter the seconds or type zeros in front of numbers.
System Date (MM:DD:YYYY)	Sets the real-time clock for the month, day, and year. Use TAB to move right; SHIFT + TAB to move left. The ENTER key may be used to move from one field to the next. The numeric keys, 0-9, are used to change the field values. It is not necessary to type zeros in front of numbers.
Diskette A or B	Selects the floppy disk drive installed in your system.

Option	Description
IDE Primary Master IDE Primary Slave IDE Secondary Master IDE Secondary Slave	These items show the IDE configuration and allow entry into the IDE sub-menus.
System Memory	Displays the amount of conventional memory detected during boot-up. This field is not user configurable.
Extended Memory	Displays the amount of extended memory detected during boot-up. This field is not user configurable.
Cache RAM	Displays the amount of cache detected and allows entry into the cache submenu.

IDE Submenu

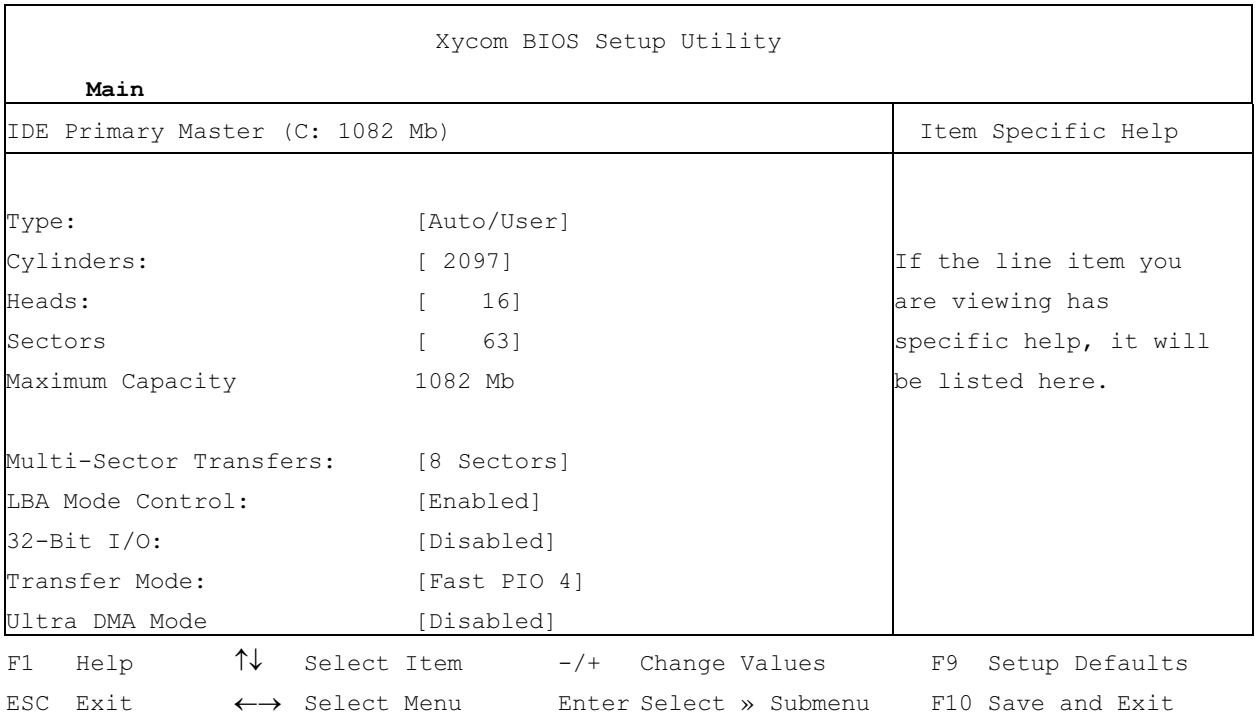
Xycom BIOS Setup Utility
Main
IDE Primary Master (C: 1082 Mb)
Item Specific Help
Type: [Auto/User]
* Cylinders: [2097]
* Heads: [16]
* Sectors [63]
* Maximum Capacity 1082 Mb
* Multi-Sector Transfers: [8 Sectors]
* LBA Mode Control: [Enabled]
* 32-Bit I/O: [Disabled]
* Transfer Mode: [Fast PIO 4]
* Ultra DMA Mode [Disabled]
If the line item you are viewing has specific help, it will be listed here.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Save and Exit

Figure 3-2. IDE Adapter Submenu

The IDE submenus are used to configure IDE hard drive information. If only one drive is attached to an IDE adapter, then only the parameters in the Master Submenu need to be entered. If two drives are connected, both Master and Slave Submenu parameters will need to be entered. All IDE submenus contain the same information and operate the same.

Table 3-2. IDE Adapter Submenu Options

Option	Description
Type	Options include Auto, None, CD-ROM, other ATAPI, and User. “Auto” autotypes at each boot. “None” indicates no device is attached. “CD-ROM” indicates that a CD-ROM drive is attached. “Other ATAPI” indicates that a removable disk drive is attached. “User” allows the user to specify device parameters.
[1, 2] Cylinders	Indicates the number of cylinders on the hard drive. This information is automatically entered if Type is set to “Auto.”

Option	Description
[1, 2] Heads	Indicates the number of read/write heads on the hard drive. This information is automatically entered if Type is set to “Auto.”
[1, 2] Sectors	Indicates the number of sectors per track on the hard drive. This information is automatically entered if Type is set to “Auto.”
[1] Maximum Capacity	Indicates the maximum storage capacity of the drive.
[3, 4] Multi-Sector Transfers	Sets the number of sectors per block. Options are Auto, 2, 4, 8, or 16 sectors. “Auto” sets the number of sectors per block to the highest number supported by the drive.
[3, 4] LBA Mode Control	Enables Logical Block Access. The default is disabled and should work with most hard drives.
[3] 32-Bit I/O	Enables 32-bit communication between CPU and IDE interface.
[3, 4] Transfer Mode	Selects the method for transferring the data between the hard disk and system memory. The drive type and cable length determine available options.
[3, 4] Ultra DMA Mode	Enables or disables the maximum storage capacity of the drive.

1 = Visible only when type is “Auto” or “User”

2 = Editable only when Type is “User”

3 = Not visible when Type is set to “None”

4 = Not editable when Type is set to “Auto”

Cache Submenu

```
                        Xycom BIOS Setup Utility
      Main
Memory Cache                                        Item Specific Help

Memory Cache:                  [Enabled]            If the line item you
Cache System BIOS area:        [Write Protect]      are viewing has
Cache Video BIOS area:         [Write Protect]      specific help, it will
Cache Base 0-512K              [Write Back]         be listed here.
Cache Base 512K-640K:          [Write Back]
Cache Extended Memory          [Write Back]
Area:
Cache Extended Memory Re-
gion
    CC00-CFFF                  [Disabled]
    D000-D3FF                  [Disabled]
   D400-D7FF                   [Disabled]
   D800-DBFF                   [Disabled]
   DC00-DFFF                   [Disabled]

F1   Help      ↑↓  Select Item      -/+   Change Values      F9  Setup Defaults
ESC  Exit      ←→  Select Menu      Enter Select » Submenu   F10 Save & Exit
```

Figure 3-3. Memory Cache Submenu

Enabling cache increases CPU performance by holding data most recently accessed in a special high-speed static RAM area called cache. The AHIP-370 provides two levels of cache memory; level one is 16 K

internal to the Pentium processor, and level two, or external cache, is the cache-on-a-stick site (COAST) which can accommodate 256 or 512 K of high-speed cache memory.

Table 3-3. Memory Cache Submenu Options

Option	Description
Memory Cache	Controls the state of Pentium II memory cache.
Cache System BIOS Area	Allows the system BIOS memory area to be cached if enabled. Enabling also increases system performance. The default is enabled and write protected.
Cache Video BIOS Area	Allows the video BIOS memory area to be cached if enabled. Enabling also increases system performance. The default is enabled and write protected.
Cache 0 - 512K	Controls caching of 512K base memory. Default is Write Back Caching.
Cache 512K - 640K	Controls caching of 512K and 640K base memory. Default is Write Back Caching.
Cache Extended Memory Area	Controls caching of system memory above 1 MB. Default is Write Back Caching.
Cache Memory Region	Caches the corresponding memory when enabled. Memory in this area is usually extended BIOS or AT-bus memory. Enabling cache may increase system performance, depending on how the extended BIOS is accessed. The default is disabled.

Advanced Menu

Figure 3-4. Advanced Setup Menu

```
                        Xycom BIOS Setup Utility
    Main      Advanced      Security      Exit
                                                    Item Specific Help
►I/O Device Configuration
►Advanced Chipset Control
►PCI Configuration                                  If the item you are
                                                    viewing has specific
Installed O/S:                  [other]             help, it will
Reset Configuration Data:       [No]                be listed here.

Large Disk Access Mode:         [DOS]
Local Bus IDE adapter:          [Both]
Floppy check:                   [Disabled]
Summary Screen:                 [Disabled]
Boot-time Diagnostic Screen     [Enabled]

►On-board Socket Site:
►Flat Panel
F1   Help      ↑↓   Select Item      -/+   Change Values      F9  Setup Defaults
ESC  Exit      ←→   Select Menu      Enter Select » Submenu   F10 Previous Values
```

This menu allows you to change the peripheral control, advanced chipset control, and disk access mode.

Table 3-4. Advanced Menu Option

Feature	Description
I/O Device Configuration	Allows entry into the I/O submenu.
Advanced Chipset Control	Allows entry into the chipset submenu.
Installed O/S	Select "Win95" if you are using an operating system with Plug & Play capabilities. Default is [Other].
Reset Configuration Data	Used to reset the Plug & Play configuration data table when new devices are added/removed or whenever the BIOS is upgraded.
Large Disk Access Mode	Select “DOS” if your system has DOS. Select “Other” if you have another operating system, such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.
Local Bus IDE Adapter	Controls configuration of local bus IDE adapter. Default is [Both] (primary and secondary).
On-board Socket Site	Allows entry into socket site submenu.
Flat Panel	Allows entry into flat panel submenu.

I/O Device Configuration Submenu

```
                        Xycom BIOS Setup Utility
                    Advanced
I/O Device Configuration                        Item Specific Help
COM A:                      [Auto]
Base I/O Address            [3F8]               If the item you
Interrupt                   [IRQ4]              are viewing has
                                                specific help, it will
COM B:                      [Auto]              be listed here.
Mode:                       [Normal]
Base I/O Address            [2F8]
Interrupt                   [IRQ3]

Parallel port:              [Auto]
Mode                        [Bi-directional]
Base I/O Address:           [378]
Interrupt                   [IRQ7]

Floppy Disk Controller      [Enabled]
Base I/O Address            [Primary]

F1   Help      ↑↓  Select Item     -/+   Change Values      F9  Setup Defaults
ESC  Exit      ←→  Select Menu     Enter Select » Submenu   F10 Previous Values
```

Figure 3-5. Integrated Peripherals Submenu

The I/O Device Configuration submenu is used to configure the COM ports, parallel ports, and enable/disable the diskette and enhanced IDE controllers.

Table 3-5. Integrated Peripherals Submenu Options

Option	Description
COM A	Allows the COM A port to be enabled, disabled, or autoselected.
COM B	Allows the COM B port to be enabled, disabled, or autoselected.
Parallel Port	Allows the parallel port to be enabled, disabled, or autoselected.
Floppy Disk Controller	Allows the floppy drive controller to be enabled, disabled, or autoselected.
[1]Base I/O Address	Select a unique address for the corresponding peripheral.
[1]Interrupt	Select an interrupt request for the corresponding peripheral.
[1]Mode	Controls the protocol for the corresponding peripheral.

1 = Visible only when corresponding peripheral is “Enabled”

Advanced Chipset Control Submenu

```
                        Xycom BIOS Setup Utility
                  Advanced
Advanced Chipset Control                          Item Specific Help

Enable Memory Gap              [Disabled]         If the item you
ECC Config:                    [Disabled]         are viewing has
SERR Signal Condition:         [Multiple bit]     specific help, it will
8-bit I/O Recovery:            [3.5]              be listed here.
16-bit I/O Recovery:           [3.5]

F1   Help      ↑↓   Select Item      -/+   Change Values      F9  Setup Defaults
ESC  Exit      ←→   Select Menu      Enter Select » Submenu   F10 Save & Exit
```

Figure 3-6. Advanced Chipset Control Submenu

This menu allows you to change the values in the chipset registers and optimize your system’s performance.

Note

Most system configurations will work best with these options in their default configurations. Fast processors may cause I/O failures at the default recovery values. You can increase the number of cycles when encountering this problem; however, slowing down the clock too much may cause I/O initialization problems. You should increase the number of clock cycles incrementally, until you see an improvement in I/O performance.

Table 3-6. Advanced Chipset Control Submenu Options

Option	Description

Enable Memory Gap	Allows creation at a 128K memory gap in conventional memory from 512K to 640K, or a 1MB memory gap in extended memory from 15 MB to 16 MB. Requires use of conventional or extended memory. Default is [Disabled].
ECC Configuration	Allows configuration of Error Checking and Correction Memory. Requires ECC memory. Default is [Disabled]
SERR Signal Conditions	Allows configuration of conditions upon which the SERR signal is to be asserted for ECC memory. Requires ECC memory. Default is [Multiple bit].
8-bit I/O Recovery	Number of ISA clock cycles inserted between back-to-back I/O operations.
16-bit I/O Recovery	

On-board Socket Site Submenu

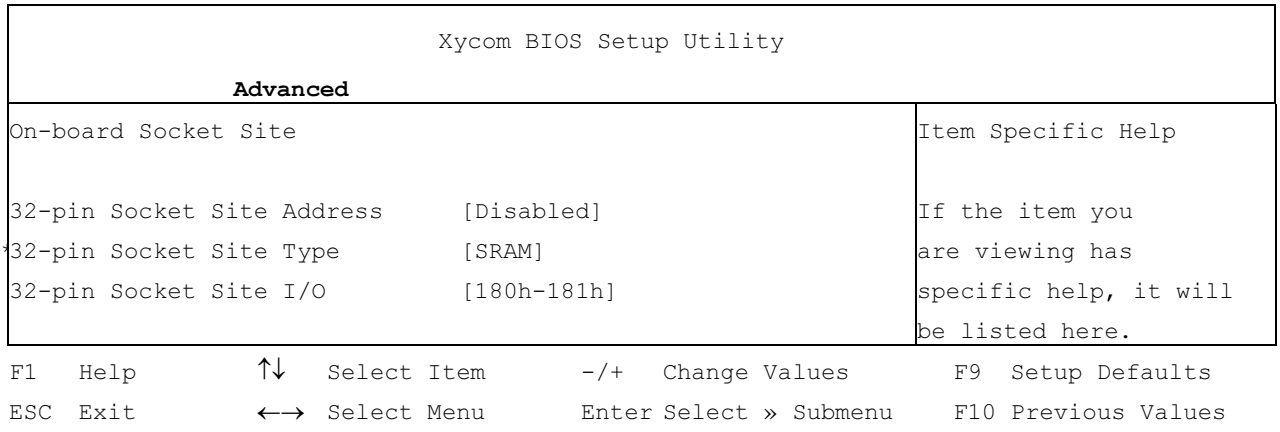
Xycom BIOS Setup Utility
Advanced
On-board Socket Site
Item Specific Help
32-pin Socket Site Address [Disabled]
*32-pin Socket Site Type [SRAM]
32-pin Socket Site I/O [180h-181h]
If the item you are viewing has specific help, it will be listed here.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Previous Values

Figure 3-7. On-board Socket Site submenu

Table 3-7. On-board Socket Site submenu options

Option	Description
32-pin Socket Site Address	Allows on-board 32-pin socket site to be disabled or mapped to a memory range. Default is [Disabled].
[1]32-pin Socket Site Type	Indicates type of memory installed in on-board 32-pin socket site. Default is [SRAM].
32-pin Socket Site I/O	Allows configuration of I/O address used by on-board 32-pin socket site. Default is [180h-181h].

1 = Visible only when Socket Site Address is “Enabled”

Flat Panel Submenu

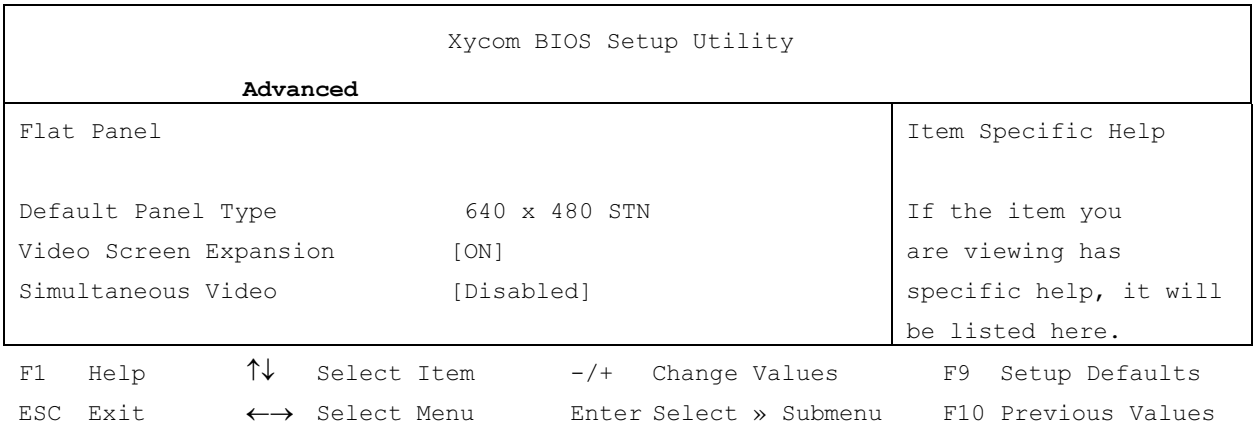

Figure 3-8. Flat Panel submenu

Table 3-8. On-board Socket Site submenu options

Option	Description
Default Panel Type	Displays video BIOS configuration. Not editable. Automatically updates when flat panel changes.
Video Screen Expansion	Enables video screen expansion to fill the area of the flat panel screen. Used most for DOS, the setting for each option depends on the type of flat panel attached to the unit. “ON” maximizes expansion as allowed for the panel, while “OFF” minimizes expansion as allowed for the panel.
Simultaneous Video	Select “Enabled” if you want video on an external CRT monitor and on the unit’s flat panel display. Select “Disabled” if you want only the flat panel display. Not editable if default panel type does not support simultaneous video.

Security Menu

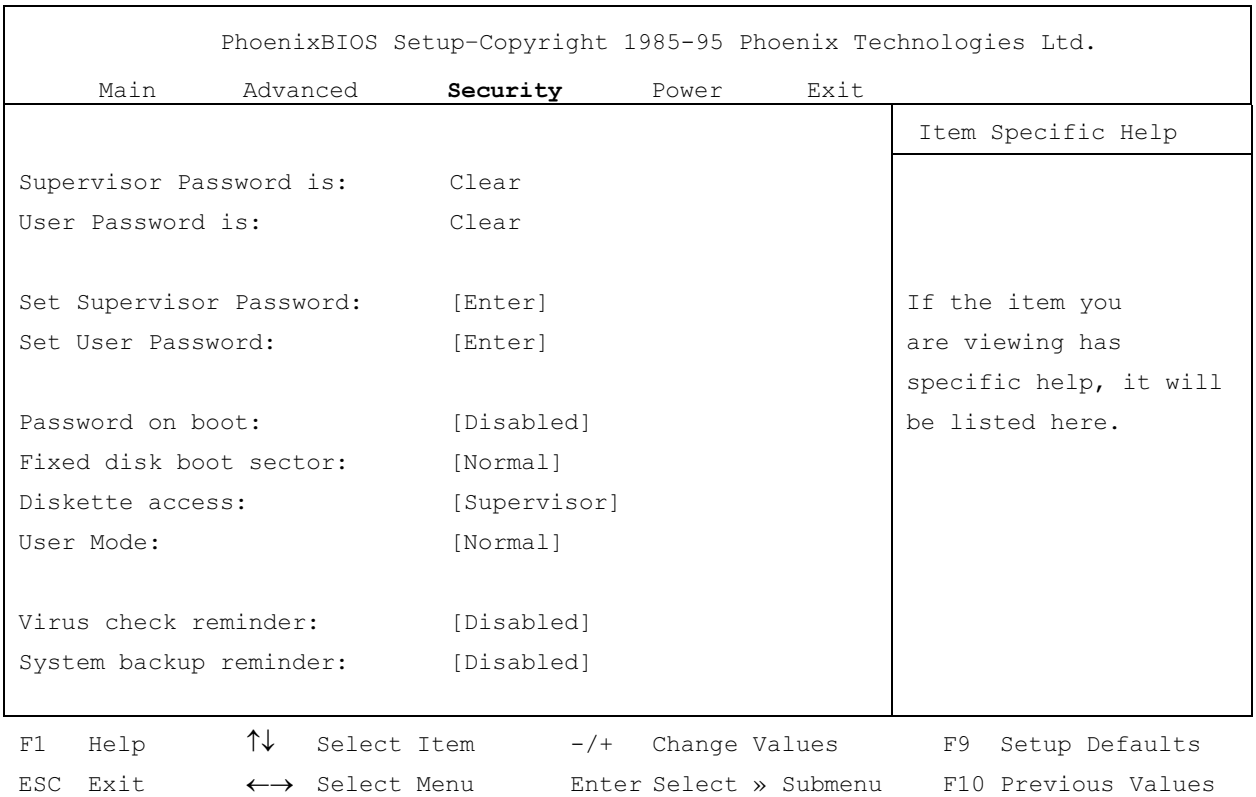
PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
Main Advanced Security Power Exit
Item Specific Help
Supervisor Password is: Clear
User Password is: Clear
Set Supervisor Password: [Enter]
Set User Password: [Enter]
Password on boot: [Disabled]
Fixed disk boot sector: [Normal]
Diskette access: [Supervisor]
User Mode: [Normal]
Virus check reminder: [Disabled]
System backup reminder: [Disabled]
If the item you are viewing has specific help, it will be listed here.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Previous Values

Figure 3-9. Security Menu

Use this menu to define system passwords and set other security options. If you change the supervisor or user password, you must enter the password a second time for verification. Passwords can prevent access to setup menus or unauthorized booting of the unit. If you use the supervisor password, you can also change the user password.

Table 3-9. Security Menu Options

Option	Description
Supervisor Password	Displays status of supervisor password. The supervisor password provides full access to setup menus.
User Password	Displays status of user password. The user password provides limited access to setup menus. The User Mode field (see below) defines access.
Set Supervisor Password	Enter the new password twice to set it. You may use up to eight alphanumeric characters. You can set the password to nothing by hitting a carriage return.
Set User Password	Enter the new password twice to set it. You may use up to eight alphanumeric characters. You can set the password to nothing by hitting a carriage return.
Password on Boot	If the supervisor password is set and this option is disabled, BIOS assumes the user is booting.
Fixed Disk Boot Sector	Write protects the disk boot sector to help prevent viruses.

Option	Description
Diskette Access	Restricts access to floppy drives to the supervisor when set to "Supervisor." Requires setting the Supervisor password.
User Mode	Defines "User" access as [Normal] or [Restricted]. In normal mode you can access the data/time, user password, power, 32-pin socket, flat panel, boot order, and disk setup settings. In restricted mode you can only access the date/time and the user password settings.
Virus Check Reminder /System Backup Reminder	Displays a message during boot up asking (Y/N) if you have backed-up the system or scanned it for any viruses. It displays the message daily on the first boot of the day; weekly on the first boot after Sunday; and monthly on the first boot of the month.

Power Menu

```
                PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
     Main      Advanced      Security      Power      Exit
                                                              Item Specific Help
   Power Savings:              [Disabled]
 * Standby Timeout:            [Off]                         If the item you
 * Suspend Timeout:            [Off]                         are viewing has spe-
                                                              cific help it would
   ▶Device Monitoring                                         be listed here.
   F1   Help      ↑↓  Select Item      -/+   Change Values      F9  Setup Defaults
   ESC  Exit      ←→  Select Menu      Enter Select » Submenu   F10 Previous Values
```

Figure 3-10. Power Menu

Table 3-10. Power Menu Options

Option	Description
Power Savings	Enables or disables power management. Options include disabled, maximum power, performance, and customized. The customized option may be used to individually set standby timeout, suspend timeout, standby CPU speed, fixed disk timeout, and CRT values.
[1]Standby Timeout	Sets an inactivity period required to put your system in standby (partial power shutdown).
[1]Suspend Timeout	Sets an inactivity period required after standby to suspend (maximum power shutdown).
Device Monitoring	Allows entry into the device configuration submenu.

1 = Visible only when power saving is "Customized"

Device Monitoring Submenu

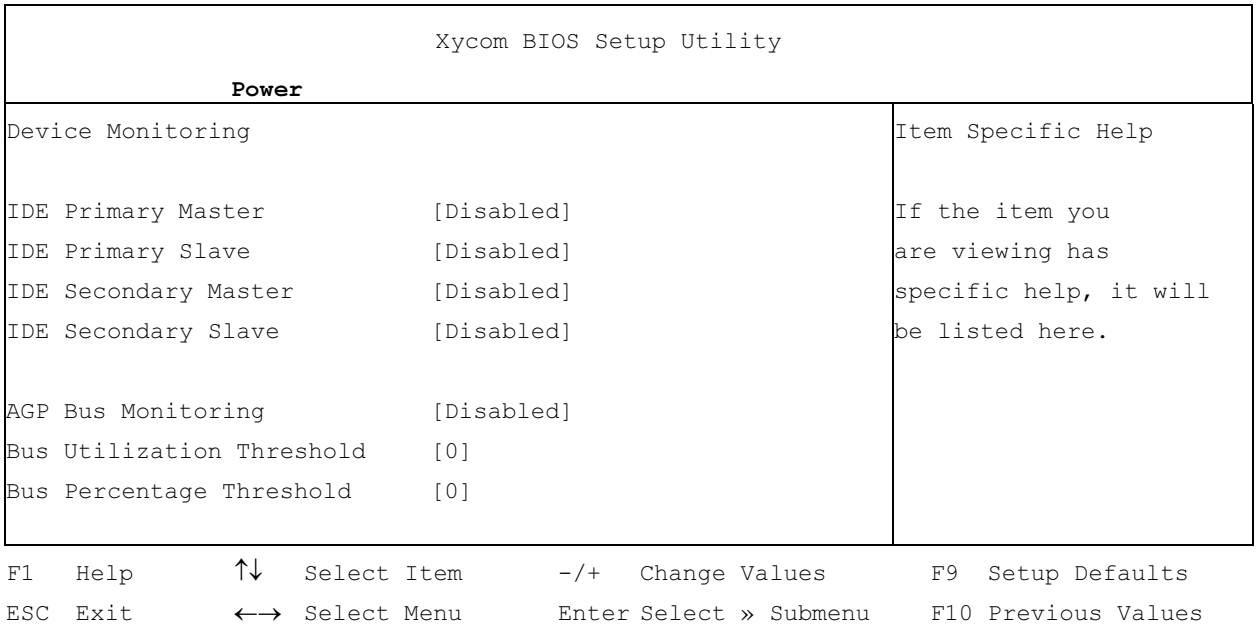
Xycom BIOS Setup Utility
Power
Device Monitoring
Item Specific Help
IDE Primary Master [Disabled]
IDE Primary Slave [Disabled]
IDE Secondary Master [Disabled]
IDE Secondary Slave [Disabled]
AGP Bus Monitoring [Disabled]
* Bus Utilization Threshold [0]
* Bus Percentage Threshold [0]
If the item you are viewing has specific help, it will be listed here.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Previous Values

Figure 3-11. Integrated Peripherals Submenu

The Device Monitoring submenu allows you to control the system's power saving features by defining how device activity will affect suspend mode.

Table 3-11. Integrated Peripherals Submenu Options

Option	Description
IDE Primary Master	When enabled, activity on the corresponding device will keep the system from entering suspend mode. Default is [disabled]. If you enable this option for an IDE CD-ROM and use an operating system, such as Windows® 95, that has an autorun feature for CDs, your system will never enter suspend mode, because the autorun feature constantly monitors the CD-ROM drive.
IDE Primary Slave	
IDE Secondary Master	
IDE Secondary Slave	
AGP Bus Monitoring	When enabled, activity on the AGP bus will keep the system from entering suspend mode. Default is [disabled].
[1]Bus Utilization Threshold	Since the AGP bus is always active, these fields allow you to set a threshold for AGP monitoring to use. These threshold settings will specify how much AGP activity must exist to prevent the system from entering suspend mode.
[1]Bus Percentage Threshold	

1 = Visible only when AGP bus monitoring is "Enabled"

Boot

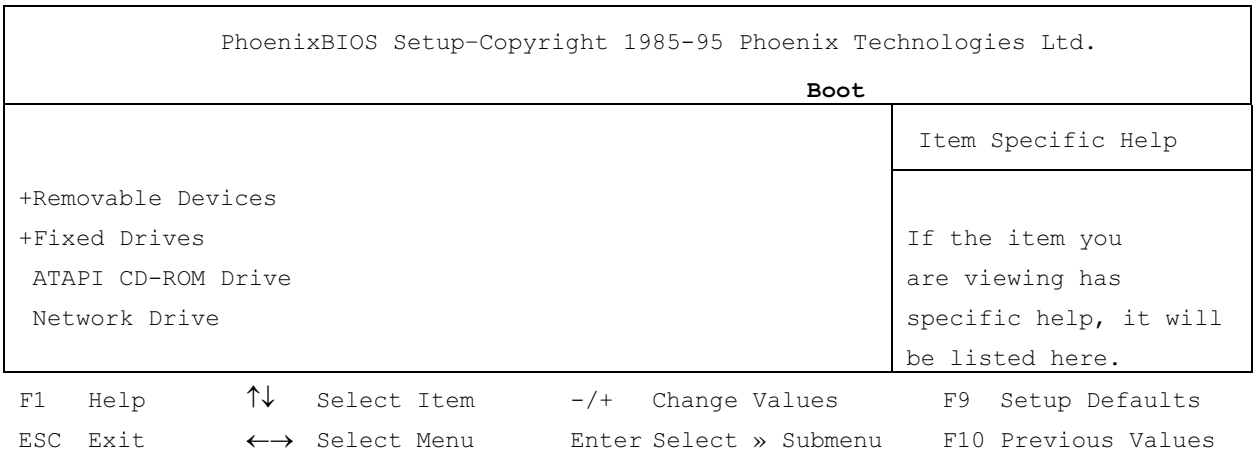
PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
Boot
Item Specific Help
+Removable Devices
+Fixed Drives
ATAPI CD-ROM Drive
Network Drive
If the item you are viewing has specific help, it will be listed here.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Previous Values

Figure 3-12. Boot Menu

This menu allows you to specify the boot order for the unit. When you power the unit up, it will attempt to boot off each of the listed devices, starting at the first device. To change this order, select items with the arrow keys and move them up or down the list with the <+> (up) and <–> (down) keys. A moveable item may be a single device or a group of devices.

The removable and fixed drives are device groups that may contain more than one device. You can change the listed order of devices in a group with the <+> (up) and <–> (down) keys, but the system will only attempt to boot off the first listed device in a group before it continues through the boot order.

You can toggle between viewing or not viewing the devices in a group by selecting the group and pressing <Enter>, and you can press <Ctrl Enter> to view all devices in all groups. ATAPI removable devices, such as LS120 or Iomega IDE Zip® drives, may appear under either the removable or fixed groups. You can move these devices between the groups by selecting them and pressing the <n> key.

Note

Anytime the configuration data (see Figure 3-4 and Table 3-4) is reset, the boot order resets to the default settings.

Exit Menu

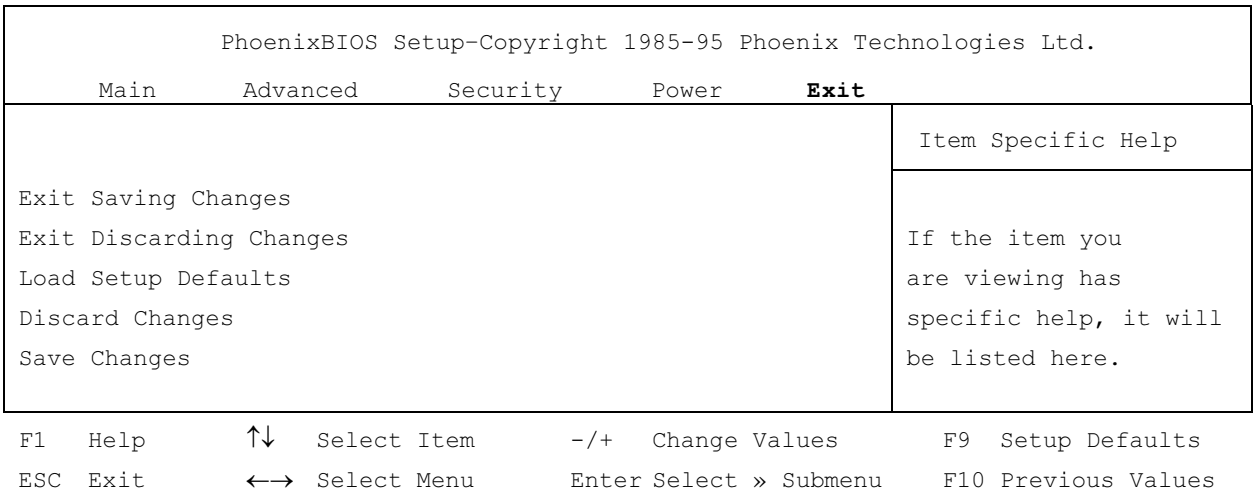
PhoenixBIOS Setup-Copyright 1985-95 Phoenix Technologies Ltd.
Main Advanced Security Power Exit
Item Specific Help
Exit Saving Changes
Exit Discarding Changes
Load Setup Defaults
Discard Changes
Save Changes
If the item you are viewing has specific help, it will be listed here.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select » Submenu F10 Previous Values

Figure 3-13. Exit Menu

This menu serves as the exit point for the setup menus. You can save the current configuration, restore the previous configuration, or load the default configuration.

Saved items are stored in battery backed CMOS RAM. The next time you boot your computer, the BIOS configures your system according to the setup selections stored in CMOS. If those values cause the system boot to fail, reboot and press F2 to enter setup. In setup, you can get the default values (as described below) or try to change the selections that caused the boot to fail.

Table 3-12. Exit Menu Options

Option	Description
Exit Saving Changes	Use this option to save the current configuration and exit.
Exit Discarding Changes	Use this option to exit Setup without storing any new selections you may have made in CMOS. The selections previously in effect remain in effect. If you have changed some items, the program asks if you want to save before exiting.
Load Setup Defaults	Use this option to load the default values for all setup items. You can return to the other menus if you want to review and change your selections. The default values are not in effect until the configuration is saved.
Discard Changes	Use this option to discard all changes since the configuration last changed (i.e., this option loads previous configuration). You can return to the other menus if you want to review and change your selections. The default values are not in effect until the configuration is saved.
Save Changes	Use this option to save all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

BIOS Compatibility

This BIOS is IBM PC/AT compatible with additional CMOS RAM and BIOS data areas used.

Appendix A- DRAM Installation

The AHIP-370 has a two 168-pin DIMM sockets in which to add memory. Due to the CPU speed, SRAM access time should be 100 MHz and must be 60 ns to run with faster SDRAM.

SDRAM sizes of 32, 64, 128, and 256 MB may be used to accommodate 100 MHz FSB.

Recommended manufacturers for SDRAM, along with the respective part numbers, are listed below.

Table A-1. 4M x 64 Part Numbers (32 meg)

Manufacturer	Part Number 100 MHz SFRAM PC100
Micron	MT16LSDT464AG-10BC4
Toshiba	THMY6440FIBEG-80H
Simple Tech	STI644106UD2-10DVG
Celestica	CLAG052QLBC000
Xycom	128668

Table A-2. 8M x 64 Part Numbers (64 Meg)

Manufacturer	Part Number SDRAM PC100
Toshiba	THMY6480FIBEG-80H
Micron	MT8LSDT864AG-10BD2
Simple Tech	ST1648116UD1-10DVG
Celestica	CLAG064JJBC000
Xycom	128674

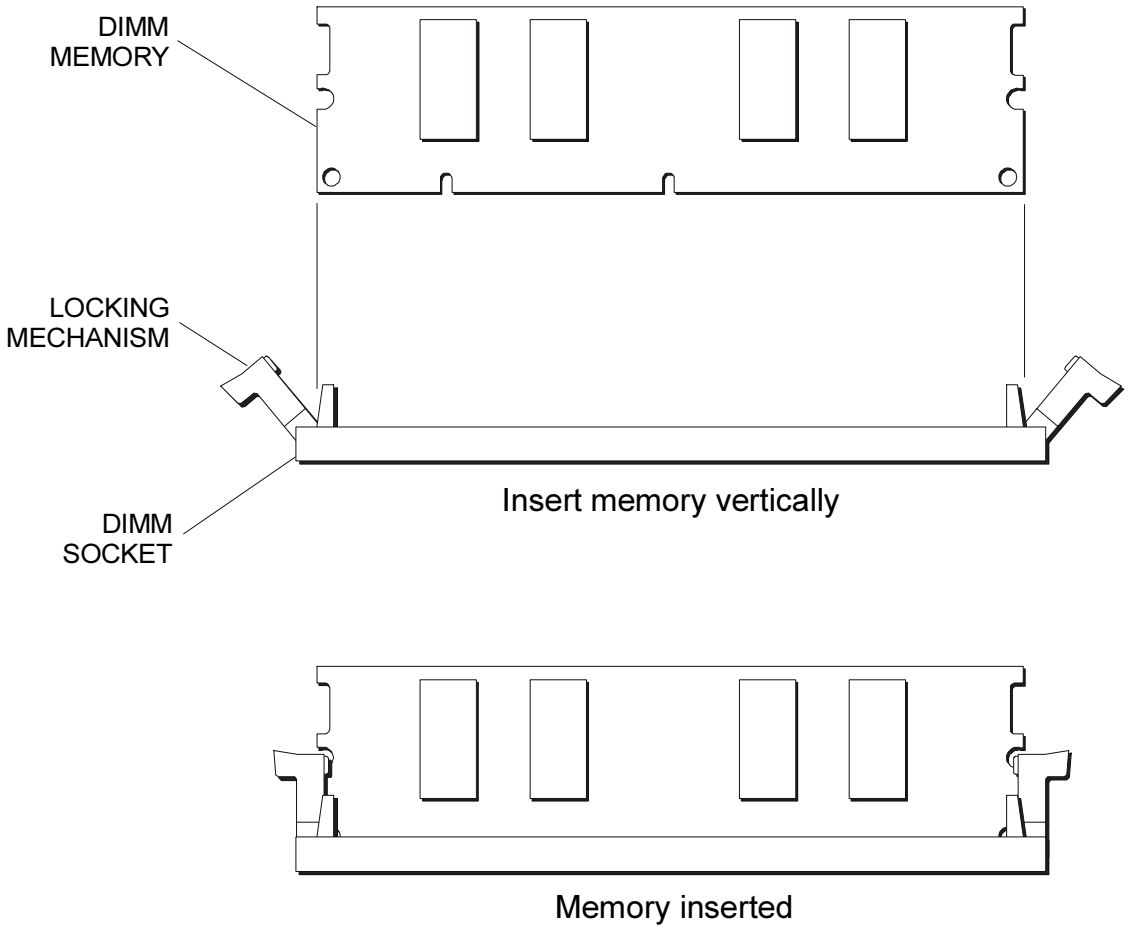

Figure A-1. SDRAM Installation

Appendix B – Video Modes

Introduction

Appendix B defines the video modes and the panels the AHIP-370 supports.

Video Modes

The Chips & Technologies 69000 VGA controller supports many standard, VESA, and extended modes. The 69000 runs in AGP, 1X mode at 66 MHz. The following tables list the standard and extended video modes and whether they passed, failed or are not supported with the CRT, TFT active color, or STN passive color displays.

Standard Modes

Mode IBM	VESA mode[1]	Number of colors	Pixels	Display mode	CRT	TFT	STN
00	-	16/256	320x200	text	OK	OK	OK
01	-	16/256	320x350	text	OK	OK	OK
02	-	16/256	640x200	text	OK	OK	OK
03	-	16/256	640x200	text	OK	OK	OK
04	-	4/256	320x200	graphics	OK	OK	OK
05	-	4/256	320x200	graphics	OK	OK	OK
06	-	2/256	640x200	graphics	OK	OK	OK
07	-	mono	720x350	text	OK	OK	OK
0D	-	16/256	320x200	graphics	OK	OK	OK
0E	-	16/256	640x200	graphics	OK	OK	OK
0F	-	mono	640x350	graphics	OK	OK	OK
10	-	16/256	640x350	graphics	OK	OK	OK
11,20	-	2/256	640x480	graphics	OK	OK	OK
12	-	16/256	640x480	graphics	OK	OK	OK
13	-	256/256	320x200	graphics	OK	OK	OK

- = Not supported by BIOS

[1] = Execute the VESA.EXE device driver to initiate VESA modes.

Extended Modes

Mode C&T	VESA Mode[a]	Number of colors	Pixels	Display mode	CRT	TFT	STN
	100	256	640x400	graphics	OK	OK	OK
30	101	256	640x480	graphics	OK	OK	OK
40	unk	32K	640x480	graphics	OK	OK	OK
41	unk	64K	640x480	graphics	OK	OK	OK
50	unk	16M	640x480	graphics	OK	OK	OK
22	102	16	800x600	graphics	OK	OK	OK
32	103	256	800x600	graphics	OK	OK	OK
42	unk	32K	800x600	graphics	OK	OK	OK
43	unk	64K	800x600	graphics	OK	OK	OK
24	104	16	1024x768	graphics	OK	OK	OK
34	unk	256	1024x768	graphics	OK	OK	OK
44	unk	32K	1024x768	graphics	OK	OK	OK
45	unk	64K	1024,768	graphics	OK	OK	OK

[a] = Execute VESA.EXE device driver to initiate VESA modes

Windows 3.1

Windows 3.1 driver (version 1.1.8)	**CRT[3]**
C&T 69000 1024x768x16	YES
1024x768x256	YES
1024x768x32K	YES
1024x768x64K	YES
1280x1024x16	YES
1280x1024x256	YES
640x480x16	YES
640x480x256	YES
640x480x32k	YES
640x480x64k	YES
640x480x16M	YES
800x600x16	YES
800x600x256	YES
800x600x32k	YES
800x600x64k	YES
800x600x16M	YES

[3] = All windows' drivers were tested on a NEC multi-sync 5FG monitor

Windows ‘95

Windows 95 driver (version 1.3.2 - included with Windows 95)	CRT[3]
C&T 69000 Display Drivers 1024x768x16	YES
1024X768X256	YES
1024X768X16bit	YES
1024x768x24bit	YES
640x480x16	YES
640x480x256	YES
640x480x16bit	YES
640x480x24bit	YES
640x480x20bit (True Color)	YES
800x600x16	YES
800x600x256	YES
800x600x16bit	YES
800x600x24bit	YES

Video Modes Supported on Windows NT	**CRT[3]**
640x480x256	YES
800x600x256	YES
1024x768x256	YES
1280x1024x256	YES
640x480x65536	YES
800x600x65536	YES
1024x768x65536	YES
640x480x16777216	YES
800x600x16777216	YES

Appendix C– Pinouts

This appendix describes the pinouts for the AHIP-370 connectors defined in Chapter 2.

VGA Connector (VGA1)

Pin	Signal
1	RED
2	GREEN
3	BLUE
4	NC
5	ORB_GND
6	ORB_GND
7	ORB_GND
8	ORB_GND
9	Fused VCC
10	ORB_GND
11	NC
12	DDCDAT
13	HSYNC
14	VSYNC
15	DDCCLK

NC = no connect

COM1 Connector RS-232/RS-485 (COM1_4)

Pin	Signal	Pin	Signal
1A	DCD1	1B	TXD-
2A	RXD1	2B	TXD+
3A	TXD1	3B	TXD TERM -
4A	DTR1	4B	TXD TERM +
5A	GND	5B	GND
6A	DSR1	6B	RXD-
7A	RTS1	7B	RXD+
8A	CTS1	8B	RXD TERM +
9A	RI1	9B	RXD TERM -

Note

'A' denotes the lower connector (RS-232) and 'B' denotes the upper connector (RS-485).

Note

For TXD termination, connect a 150Ω, ½ watt resistor from pin 3B to pin 4B, with pin 1B connected to pin 3B and pin 2B connected to pin 4B.

For RXD termination, connect a 150Ω, ½ watt resistor from pin 8B to pin 9B, with pin 6B connected to pin 9B and pin 7B connected to pin 8B.

LPT1/COM2 RS-232 Connector (PARCOM2)

Pin	Signal	Pin	Signal
1A	STROBE	1B	ORB_GND
2A	PD(0)	2B	TXD2
3A	PD(1)	3B	RXD2
4A	PD(2)	4B	RTS2
5A	PD(3)	5B	CTS2
6A	PD(4)	6B	DSR2
7A	PD(5)	7B	GND
8A	PD(6)	8B	DCD2
9A	PD(7)	9B	NC
10A	PACK	10B	NC
11A	PBUSY	11B	PB_RESET*
12A	PE	12B	NC
13A	SELECT	13B	NC

Pin	Signal	Pin	Signal
14A	AUTOFEED	14B	NC
15A	PERROR	15B	NC
16A	INIT	16B	NC
17A	SELIN	17B	NC
18A	GND	18B	NC
19A	GND	19B	NC
20A	GND	20B	DTR2
21A	GND	21B	NC
22A	GND	22B	RI2
23A	GND	23B	NC
24A	GND	24B	NC
25A	GND	25B	NC

Note

'A' denotes the lower connector (LPT1) and 'B' denotes the upper connector (COM2, RS-232). This connector also contains the remote system reset option. The reset jumper (J1) must be in position B for this option to work. The PB_RESET* pin must be switched to GND to reset the entire board.

DCIN1 Power Connector (PWR1)

Pin	Signal
1	3.3V
2	3.3V
3	GND
4	+5
5	GND
6	+5
7	GND
8	NC
9	5VSB
10	+12
11	3.3V
12	-12
13	GND
14	PSON
15	GND
16	GND
17	GND
18	-5
19	+5
20	+5

Note

-5V is not provided by the power supplies and will have to be created on the backplane board.

Touch Control Connector (TCTRL1)

Pin	Signal	Pin	Signal
1	+5V	21	GND
2	NC	22	KB_AIN0
3	+12V	23	GND
4	NC	24	KB_AIN1
5	NC	25	GND
6	-12V	26	RESET
7	NC	27	NC
8	NC	28	TXD2
9	+5V	29	NC
10	NC	30	TCH_RXD2
11	NC	31	NC
12	KB_P14	32	+5V
13	AUX_CLK	33	NC
14	AUX_DATA	34	AUX_DATA
15	H8_CLK	35	AUX_CLK
16	H8_DATA	36	UL
17	NC	37	LL
18	GND	38	SENSE
19	TCH_LED*	39	LR
20	NC	40	UR

Touch Connector (TCH1)

Pin	Signal
1	UR
2	LR
3	SENSE
4	LL
5	UL

Internal Mouse Connector (MS2)

Pin	Signal
1	GND
2	5VFUSE
3	AUX_CLK
4	AUX_DATA

Internal LED Connector (LEDMSC1)

Pin	Signal	Pin	Signal
1	5VFUSE	11	KSI(6)
2	NC	12	NC
3	5VFUSE	13	NC
4	NC	14	NC
5	GND	15	GND
6	IR_RXD2	16	COM_LED
7	TXD2	17	ALPHA_LED
8	IR_MODE	18	USER_LED
9	KSO(12)	19	IDEACTP_LED
10	KSI(7)	20	GND

LED In_Keypad Connector (LEDKB1)

Pin	Signal	Pin	Signal
1	IDEACTP_LED	6	GND
2	USER_LED	7	NC
3	ALPHA_LED	8	IR_MODE
4	COM_LED	9	TXD2
5	+5V (thru 330Ω res)	10	IR_RXD2

Flat Panel Connector (FPNL1 and FPNL2)

Pin	Signal	Pin	Signal
1	GND	31	GND
2	SHFCLK	32	P(4)
3	GND	33	P(5)
4	LP	34	P(6)
5	FLM	35	P(7)
6	GND	36	GND
7	P(16)	37	M
8	P(17)	38	VCCSW
9	P(18)	39	VCCSW
10	P(19)	40	+5V
11	GND	41	+5V
12	P(20)	42	PANEL_LOGIC
13	P(21)	43	PANEL_LOGIC
14	P(22)	44	+3.3V_CPU
15	P(23)	45	+3.3V_CPU
16	GND	46	GND
17	P(8)	47	FPSEL(0)
18	P(9)	48	FPSEL(1)
19	P(10)	49	FPSEL(2)
20	P(11)	50	FPSEL(3)
21	GND	51	+12V
22	P(12)	52	NC(Note 1)
23	P(13)	53	ENAVEE
24	P(14)	54	POT_DQ
25	P(15)	55	POT_CLK
26	GND	56	POT_RST*
27	P(0)	57	TEMP_RST*
28	P(1)	58	ENAVDD
29	P(2)	59	ENABCK
30	P(3)	60	RESET*

Backlight Inverter Connector (DCINV1)

Pin	Signal
1	+12V (switched)
2	+12V (switched)
3	Undefined Voltage
4	ENABKL (thru 10K Ω res
5	Undefined Voltage
6	Undefined Voltage
7	GND
8	GND

Internal Keyboard Connector (KYBD1)

Pin	Signal
1	KB_CLK
2	GND
3	KB_DATA
4	5VFUSE
5	SPEAKER

PS/2 Keyboard/Mouse Connector (KBMS1)

Note

If the touchscreen controller is using the mouse port, this interface will not be available.

Pin	Signal	Pin	Signal
1A	KB_DATA	1B	AUX_DATA
2A	NC	2B	NC
3A	GND	3B	GND
4A	5VFUSE	4B	5VFUSE
5A	KB_CLK	5B	AUX_CLK
6A	NC	6B	NC

Internal Floppy Connector (FDD1)

Pin	Signal	Pin	Signal
1	+5V	14	FSTEP*
2	IDX*	15	GND
3	+5V	16	FWD*
4	FDS1*	17	GND
5	+5V	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTK0*
8	NC	21	GND
9	NC	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

External Floppy Connector (FDD2)

Pin	Signal	Pin	Signal
1	+5V	14	FSTEP*
2	IDX*	15	NC
3	FDS1*	16	FWD*
4	+5V	17	GND
5	NC	18	FWE*
6	DCHG*	19	GND
7	NC	20	FTK0*
8	NC	21	GND
9	GND	22	FWP*
10	MO1*	23	GND
11	NC	24	FRDD*
12	FDIRC*	25	GND
13	NC	26	FHS*

IDE Connector (HDD1)

Pin	Signal	Pin	Signal
1	IDERESET*	21	HDRQ0
2	GND	22	GND
3	HDD7	23	HDIOW*
4	HDD8	24	GND
5	HDD6	25	HDIOR*
6	HDD9	26	GND
7	HDD5	27	HDIORDY
8	HDD10	28	ALE (pullup)
9	HDD4	29	HDAK0
10	HDD11	30	GND
11	HDD3	31	IRQ14
12	HDD12	32	HDIOCS16*
13	HDD2	33	HDA1
14	HDD13	34	NC
15	HDD1	35	HDA0
16	HDD14	36	HDA2
17	HDD0	37	HDCS0*
18	HDD15	38	HDCS1*
19	GND	39	IDEACTP*
20	NC	40	GND

ISA/IDE Backplane Connector (ATIDE1)

Pin	Signal	Pin	Signal
1	SD(7)	61	IOCHK*
2	SD(6)	62	RESETDRV
3	SD(5)	63	IRQ9
4	SD(4)	64	GND
5	SD(3)	65	DRQ2
6	SD(2)	66	0WS*
7	SD(1)	67	IOCHRDY
8	SD(0)	68	AEN
9	SA(19)	69	SMEMW*
10	SA(18)	70	SMEMR*
11	SA(17)	71	IOW*
12	SA(16)	72	IOR*
13	SA(15)	73	DACK3*
14	SA(14)	74	DRQ3
15	SA(13)	75	DACK1*
16	SA(12)	76	DRQ1
17	SA(11)	77	REF*
18	SA(10)	78	SYSCLK
19	SA(9)	79	IRQ7
20	SA(8)	80	IRQ6
21	SA(7)	81	IRQ5
22	SA(6)	82	IRQ4
23	SA(5)	83	IRQ3
24	SA(4)	84	DACK2*
25	SA(3)	85	T/C
26	SA(2)	86	BALE
27	SA(1)	87	OSC
28	SA(0)	88	SBHE*
29	LA(23)	89	MEMCS16*
30	LA(22)	90	IOCS16*
31	LA(21)	91	IRQ10
32	LA(20)	92	IRQ11
33	LA(19)	93	IRQ12
34	LA(18)	94	IRQ15
35	LA(17)	95	IRQ14
36	SD(8)	96	DACK0*
37	SD(9)	97	MEMR*
38	SD(10)	98	DRQ0
39	SD(11)	99	MEMW*
40	SD(12)	100	DACK5*
41	SD(13)	101	DRQ5
42	SD(14)	102	DACK6*
43	SD(15)	103	DRQ6
44	HDDACK0*	104	DACK7*

Pin	Signal	Pin	Signal
45	HDDRQ0	105	DRQ7
46	GND	106	MASTER16*
47	HDD(7)	107	IDERST*
48	HDD(6)	108	HDD(8)
49	HDD(5)	109	HDD(9)
50	HDD(4)	110	HDD(10)
51	HDD(3)	111	HDD(11)
52	HDD(2)	112	HDD(12)
53	HDD(1)	113	HDD(13)
54	HDD(0)	114	HDD(14)
55	HDIOW*	115	HDD(15)
56	HDIORDY	116	HDIOR*
57	IDE_IRQ	117	HDIOCS16*
58	HDA0	118	HDA1
59	HDCS0*	119	HDA2
60	IDEACTP*	120	HDCS1*

PCI Backplane Connector (PCIMG1)

Pin	Signal	Pin	Signal
1	+5V	61	-12V
2	+12V	62	GND
3	+5V	63	GND
4	+5V	64	NC
5	+5V	65	+5V
6	PIRQA*	66	+5V
7	PIRQC*	67	PIRQB*
8	+5V	68	PIRQD*
9	PCLKS3	69	REQ3*
10	+5V	70	REQ1*
11	NC	71	GNT3*
12	GND	72	GND
13	GND	73	GND
14	GNT1*	74	PCLKS2
15	AGPRST*	75	GND
16	+5V	76	PCLKS0
17	GNT0*	77	GND
18	GND	78	REQ0*
19	REQ2*	79	+5V
20	AD(30)	80	PAD(31)
21	+3.3V_CPU	81	PAD(29)
22	PAD(28)	82	GND
23	PAD(26)	83	PAD(27)
24	GND	84	PAD(25)
25	PAD(24)	85	+3.3V_CPU
26	GNT2*	86	C_BE*(3)
27	+3.3V_CPU	87	PAD(23)
28	PAD(22)	88	GMD
29	PAD(20)	89	PAD(21)
30	GND	90	PAD(19)
31	PAD(18)	91	+3.3V_CPU
32	PAD(16)	92	PAD(17)
33	+3.3V_CPU	93	C_BE*(2)
34	FRAME*	94	GND
35	GND	95	IRDY*
36	TRDY*	96	+3.3V_CPU
37	GND	97	DEVSEL*
38	STOP*	98	GND
39	+3.3V_CPU	99	PLOCK*
40	SDONE (pullup)	100	PERR*
41	SB0* (pullup)	101	+3.3V_CPU
42	GND	102	SERR*
43	PAR	103	+3.3V_CPU
44	PAD(15)	104	C_BE*(1)

Pin	Signal	Pin	Signal
45	+3.3V_CPU	105	PAD(14)
46	PAD(13)	106	GND
47	PAD(11)	107	PAD(12)
48	GND	108	PAD(10)
49	PAD(9)	109	GND
50	C_BE*(0)	110	PAD(8)
51	+3.3V_CPU	111	PAD(7)
52	PAD(6)	112	+3.3V_CPU
53	PAD(4)	113	PAD(5)
54	GND	114	PAD(3)
55	PAD(2)	115	GND
56	PAD(0)	116	PAD(1)
57	+5V	117	+5V
58	REQ64* (pullup)	118	ACK64* (pullup)
59	+5V	119	+5V
60	+5V	120	+5V

Keypad connector (KEYPAD1)

Pin	Signal	Pin	Signal
1	GND	11	KSI(7)
2	KSO(9)	12	KSO(0)
3	KSO(10)	13	KSO(1)
4	KSI(0)	14	KSO(2)
5	KSI(1)	15	KSO(3)
6	KSI(2)	16	KSO(4)
7	KSI(3)	17	KSO(5)
8	KSI(4)	18	KSO(6)
9	KSI(5)	19	KSO(7)
10	KSI(6)	20	KSO(8)

USB Connector

Pin	Description	Pin	Description
1A	GND	1B	5V Fuse
2A	USBP0+	2B	USBP1+
3A	USBP0-	3B	USBP1-
4A	GND	4B	GND

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